Partitioning Methods for Satisfiability Testing on Large Formulas *

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Abstract

A propositional satisfiability tester is needed as a subroutine for many applications in automated verification, automated theorem proving, and other fields. Such applications may generate very large formulas, some of which are beyond the capabilities of known algorithms. This paper investigates methods for partitioning such formulas effectively, to produce smaller formulas within the reach of known algorithms. CNF formula partitioning can be viewed as hypergraph partitioning, which has been studied extensively in VLSI design. Although CNF formulas have been considered as hypergraphs before, we found that this viewpoint was not productive for partitioning, and we introduce a new viewpoint in the dual hypergraph. Hypergraph partitioning technology from VLSI design is adapted to this problem. The overall goal of satisfiability testing requires criteria different from those used in VLSI design. Several heuristics are described, and investigated experimentally. Some formulas from circuit applications that were extremely difficult or impossible for existing algorithms have been solved. However, the method is not useful on formulas with little or no "structure", such as randomly generated formulas.

Keywords: Propositional logic, boolean formula, satisfiability, hypergraph partition, min-cut bisection.

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